

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Eliyahou Harari		
Title:	Flash Memory Cell Arrays Having Dual Control Gates Per Memory Cell Charge Storage Element		
Application No.:	Unassigned	Filing Date:	Herewith
Examiner:	Unassigned	Group Art Unit:	Unassigned
Docket No.:	SNDK.304US1	Conf. No.:	Unassigned

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant calls the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application. Copies of the documents listed on the accompanying Form PTO-1449 and Form PTO-892 that are not enclosed were previously submitted in Application No. 10/282,747 from which this Application claims an earlier effective filing date.

Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a representation that a search has been made (other than as indicated by any cited document), or (3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

Attorney Docket No.: SNDK.304US1
Express Mail No.: EV321705732US


Application No.: Unassigned

This information disclosure statement is submitted under 37 C.F.R. § 1.97(b) and consequently no fee should be required. The Commissioner is authorized, however, to charge any fee that may be required, or to credit any overpayment, against Deposit Account No. 502664. This form is being submitted in duplicate.

**EXPRESS MAIL
LABEL NO:**

EV321705732US

Respectfully submitted,



Gerald P. Parsons
Reg. No. 24,486

March 1, 2004

Date

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Eliyahou Harari

Assignee: SanDisk Corporation

Title: Flash Memory Cell Arrays Having Dual Control Gates Per Memory Cell Charge Storage Element

Application No.: 10/282,747

Filing Date: October 28, 2002

Examiner: Unassigned

Group Art Unit: 2811

Docket No.: M-12879 US

Conf. No.: 7200

COPY

San Francisco, California
January 14, 2003

Box Missing Parts
Commissioner for Patents
Washington, D. C. 20231

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR § 1.97(b)**

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

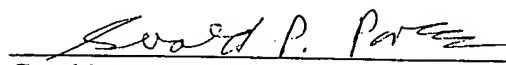
Citation of these documents shall not be construed as:

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EXPRESS MAIL LABEL NO:

EV259164530US

Respectfully submitted,


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U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Application No.	
				M-12879 US		10/282,747	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant			
(Use several sheets if necessary)				Eliyahou Harari			
COPY				Filing Date		Group	
				October 28, 2002		2811	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	1	5,043,940	Aug. 27, 1991	Harari			
	2	5,095,344	Mar. 10, 1992	Harari			
	3	5,172,338	Dec. 15, 1992	Mehrotra et al.			
	4	5,343,063	Aug. 30, 1994	Yuan et al.			
	5	5,570,315	Oct. 29, 1996	Tanaka et al.			
	6	5,677,872	Oct. 14, 1997	Samachisa et al.			
	7	5,774,397	Jun. 30, 1998	Endoh et al.			
Foreign Patent Documents							
							Translation
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
	8	Chan et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device", IEEE Electron Device Letters, Vol. EDL-8, No. 3, March, 1987, pp. 93-95.					
	9	Nozaki et al., "A 1-Mb EEPROM With MONOS Memory Cell for Semiconductor Disk Application", IEEE Journal of Solid-State Circuits, Vol. 26, No. 4, April 1991, pp. 497-501.					
	10	Choi et al., "A Novel Booster Plate Technology in High Density NAND Flash Memories for Voltage Scaling-Down and Zero Program Disturbance", IEEE Symposium on VLSI Technology Digest of Technical Papers, 1996, pp. 238-239.					
	11	Kim et al., "Fast Parallel Programming of Multi-Level NAND Flash Memory Cells Using the Booster-Line Technology", Symposium on VLSI Technology Digest of Technical Papers, 1997, pp. 65-66.					
	12	Choi et al., "A Triple Polysilicon Stacked Flash Memory Cell With Wordline Self-Boosting Programming", IEEE, 1997, pp. 283-286.					
	13	Satoh et al., "A Novel Channel Boost Capacitance (CBC) Cell Technology with Low Program Disturbance Suitable for Fast Programming 4Gbit NAND Flash Memories", IEEE Symposium on VLSI Technology Digest of Technical Papers, 1998, pp. 108-109.					
Examiner			Date Considered				
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

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U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Application No.		
				M-12879 US		10/282,747		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant				
(Use several sheets if necessary)				Eliyahou Harari				
COPY				Filing Date		Group		
				October 28, 2002		2811		
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*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
14	5,877,980	Mar. 2, 1999	Mang et al.					
15	5,936,887	Aug. 10, 1999	Choi et al.					
16	5,990,514	Nov. 23, 1999	Choi et al.					
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19	6,093,605	Jul. 25, 2000	Mang et al.					
20	6,103,573	Aug. 15, 2000	Harari et al.					
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Foreign Patent Documents								
							Translation	
	Document	Date	Country	Class	Subclass	Yes	No	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
22	Suh et al., "A 3.3V 32Mb NAND Flash Memory With Incremental Step Pulse Programming Scheme", IEEE International Solid-State Circuits Conference, Digest of Technical Papers, February, 1995, pp. 94-95, 305-306, 128-129, and 350.							
Examiner			Date Considered					
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>								

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Notice of References Cited

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Application/Control No.

10/282,747

Applicant(s)/Patent Under

Reexamination

HARARI, ELIYAHOU

Examiner

Viet Q Nguyen

Art Unit

2818

Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0155599	08-2003	Hsu et al.	257/296
*	B	US-2004/0021171	02-2004	Nishizaka, Teichiro	257/315
*	C	US-2002/0014645	02-2002	Kobayashi, Toshio	257/296
*	D	US-6,246,607	06-2001	Mang et al.	365/185.17
*	E	US-6,069,382	05-2000	Rahim, Irfan	257/316
*	F	US-2003/0032241	02-2003	Seo et al.	438/257
*	G	US-6,108,239	08-2000	Sekariapuram et al.	365/185.28
*	H	US-2003/0227811	12-2003	Sugiura et al.	365/222
*	I	US-6,563,728	05-2003	Kobayashi, Toshio	365/63
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*	K	US-6,472,707	10-2002	Takahashi, Keita	257/315
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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.